Barcelona Supercomputing Center
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Creating an Open HPC Ecosystem with RISC-V

28/1/2022

EUM'22

Overview

- Technology Trends
- What is RISC-V?
- SIG-HPC
- Getting Started
- Q&A

Technology Trends

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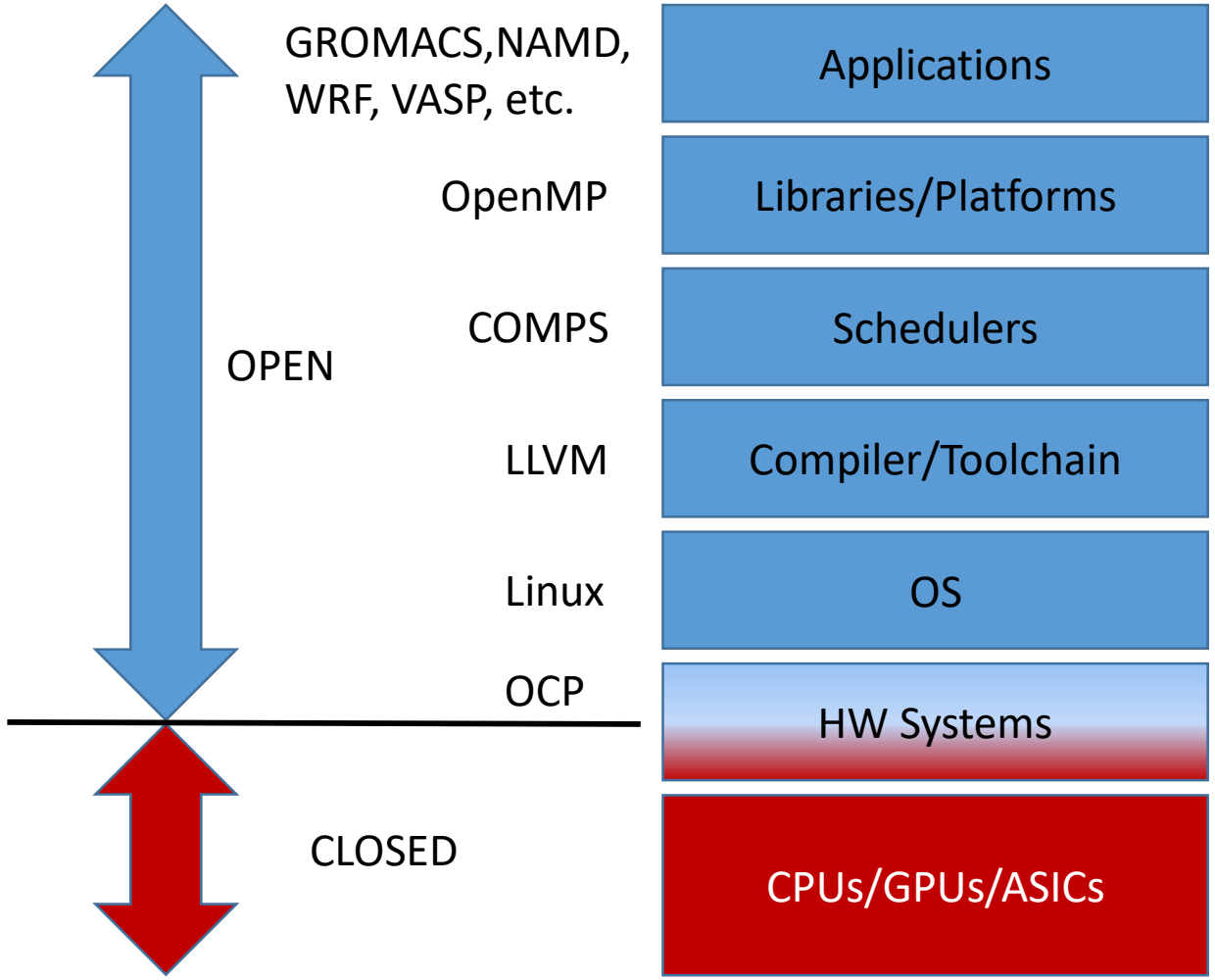
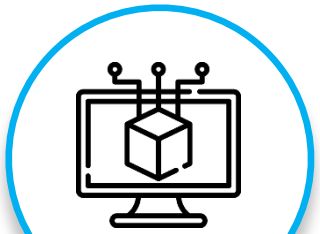
HPC Today

- **Europe has led the way in defining a common open HPC software ecosystem**
- **Linux** is the de facto standard OS despite proprietary alternatives
- Software landscape from Cloud to IoT already enjoys the benefit of open source
- Open source provides:
  - A common platform, specification and interface
  - Accelerates building new functionality by leveraging existing components
  - Lowers the entry barrier for others to contribute new components
  - Crowd-sources solutions for small and larger problems
- **What about Hardware and in particular, the CPU?**



Today´s technology trends



Massive penetration of Open Source Software

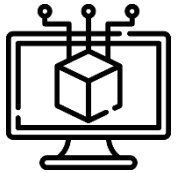
- IoT (Arduino),
- Mobile (Android),
- Enterprise (Linux),
- HPC (Linux, OpenMP, etc.)

Moore´s Law + Power = **Specialization**

- More cost effective
- More performant
- Less Power

SOFTWARE/
HARDWARE
CO-DESIGN

Today´s technology trends



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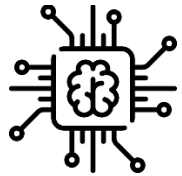
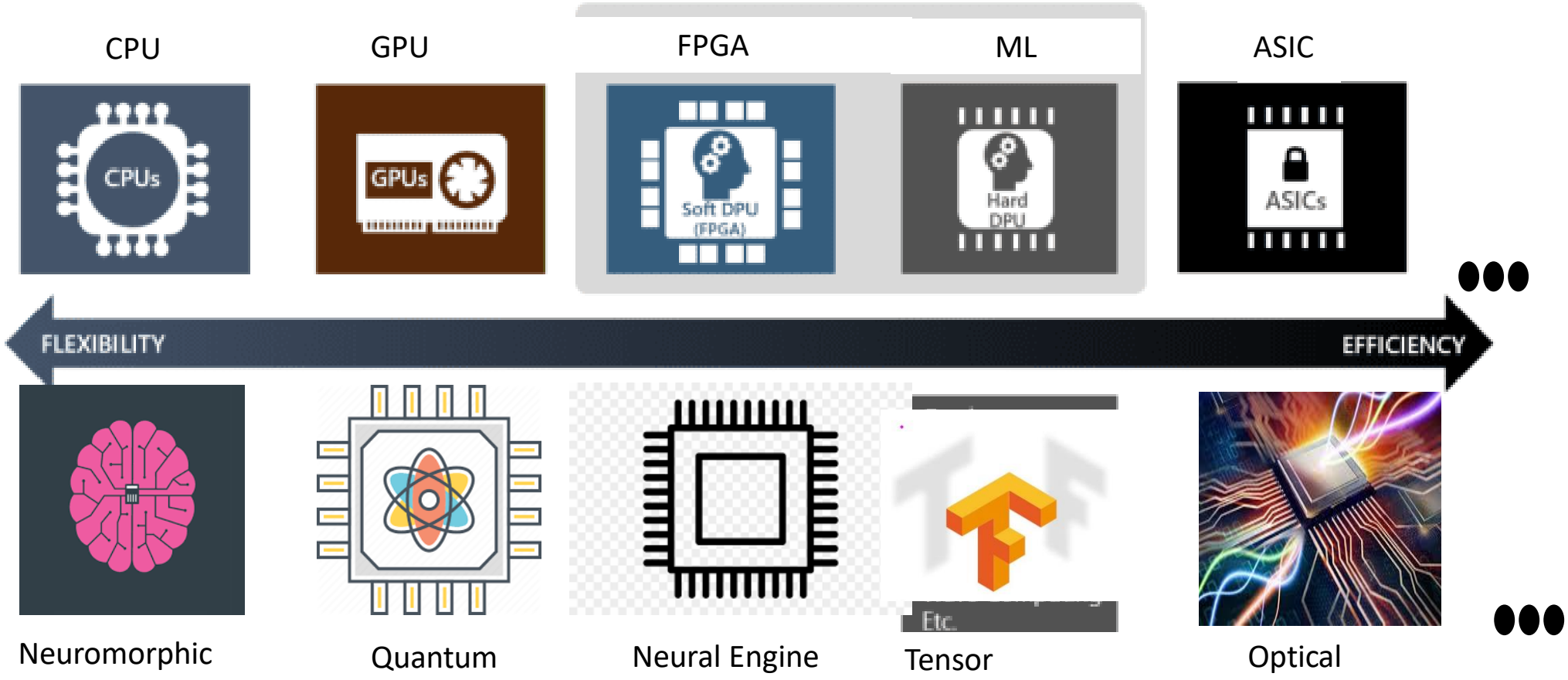


New Open Source Hardware Momentum from IoT and the Edge to HPC

- RISC-V
- OpenPOWER

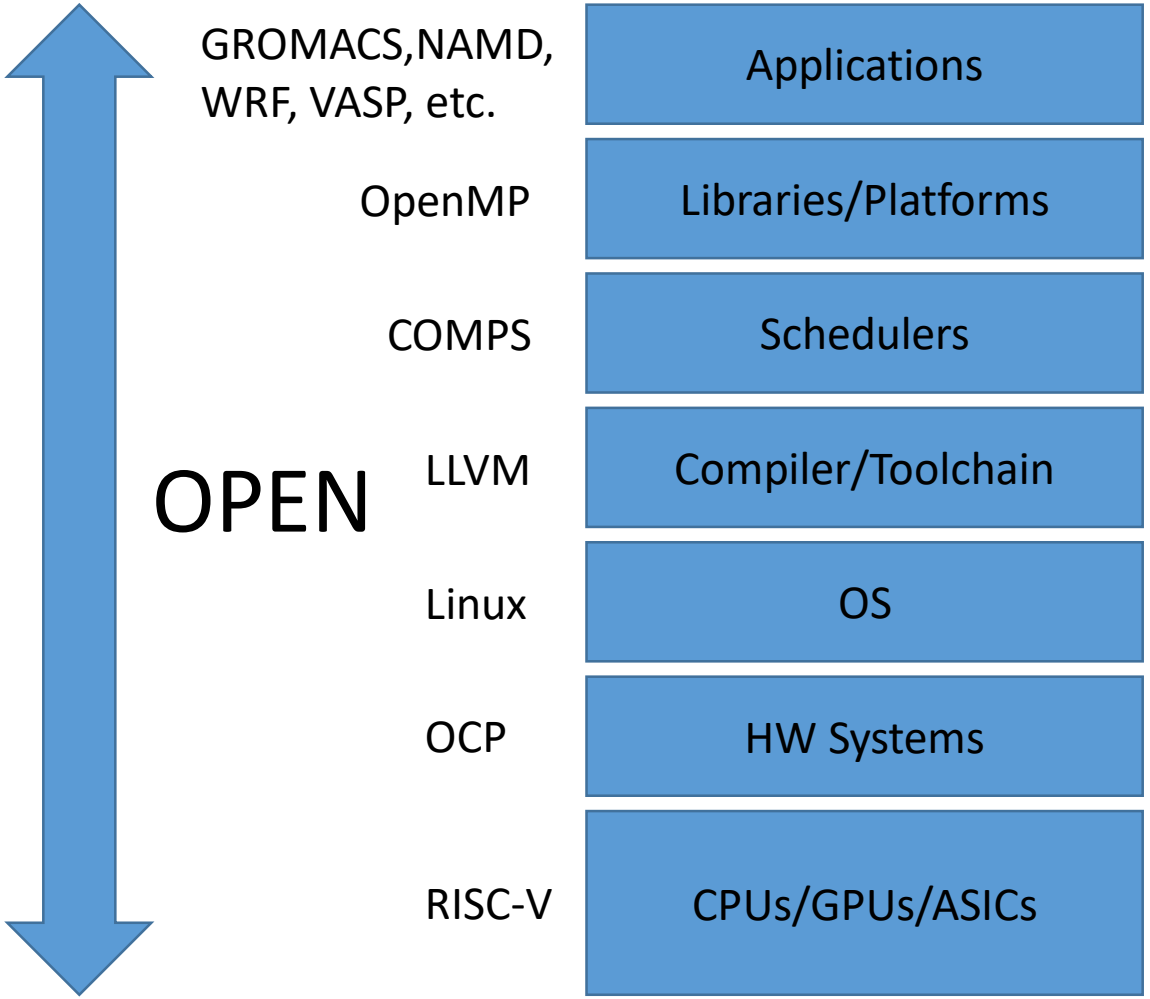
Future HPC Systems Will be Customized…

You will be able to dial up what you need in your computer for your application mix …



HPC Tomorrow

- Europe can lead the way to a completely **open SW/HW stack for the world**
- RISC-V provides the open source hardware alternative to dominating proprietary non-EU solutions
- Europe can achieve complete technology independence with these foundational building blocks
- Currently at the same early stage in HW as we were with SW when Linux was adopted many years ago
- **RISC-V can unify, focus, and build a new microelectronics industry in Europe.**



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Why Open Source Hardware?

Software: Leverage a large ecosystem compatible across implementations
Security: A fully auditable collection of IPs: processors, accelerators, etc.
Safety: No black-boxes
SWaP & Customization: SW/HW co-design for exact feature match
Performance: State-of-the-art implementations
No vendor lock-in: Ecosystem to enable custom develop from SME to large enterprise
Sovereignty: Freedom of access and implementation from design to production
Open Collaboration: Faster time to market, community, leverage existing open source

What is RISC-V?

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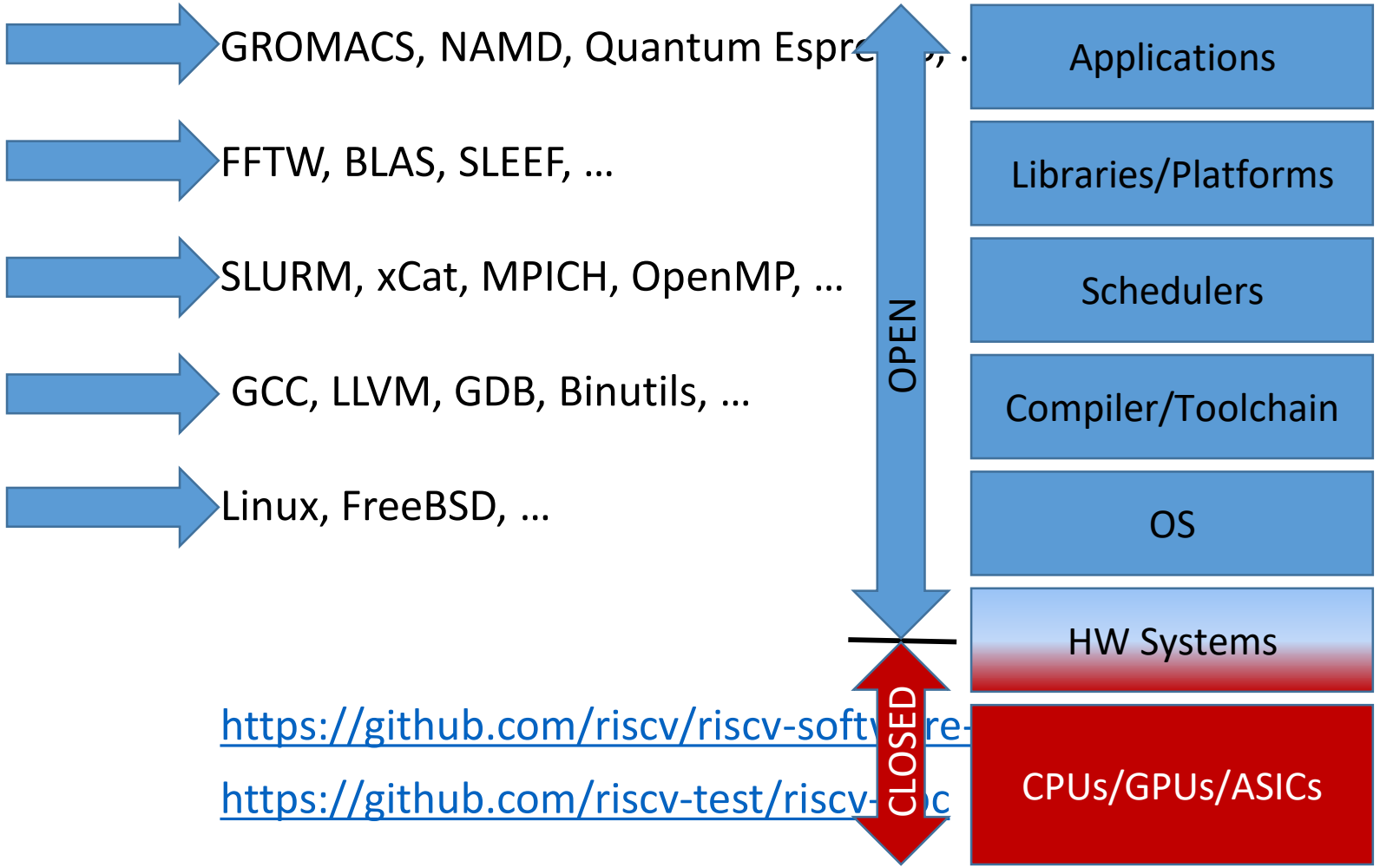
What is an ISA?

- An **Instruction Set Architecture (ISA) is part of the abstract model of a computer** that defines how the CPU is controlled by the software. The ISA acts as an interface between the hardware and the software, specifying both what the processor is capable of doing as well as how it gets done.
- The **ISA** provides the only way through which a user is able to interact with the hardware. It can be viewed as a **programmer's manual** because it's the portion of the machine that is visible to the assembly language programmer, the compiler writer, and the application programmer.
- The **ISA defines the supported data types, the registers, how the hardware manages main memory, key features (such as virtual memory), which instructions a microprocessor can execute, and the input/output model** of multiple ISA implementations. The ISA can be extended by adding instructions or other capabilities, or by adding support for larger addresses and data values.
- CPUs/devices that execute the instructions are an implementation of the ISA
  - ARM, MIPS, SPARC, Power, OpenPOWER, **RISC-V**, x86, etc…

RISC-V History

- 2010: Started development and initial proposal @ UC Berkeley
- 2015: RISC-V Foundation formed
- 2019: Adopted by many major companies
  - Starting in the embedded market with already over 1 Billion CPUs
  - RISC-V Foundation moves to Switzerland
- 2021:
  - 2B+ Cores shipped

Open Ecosystem HW/SW Co-Design



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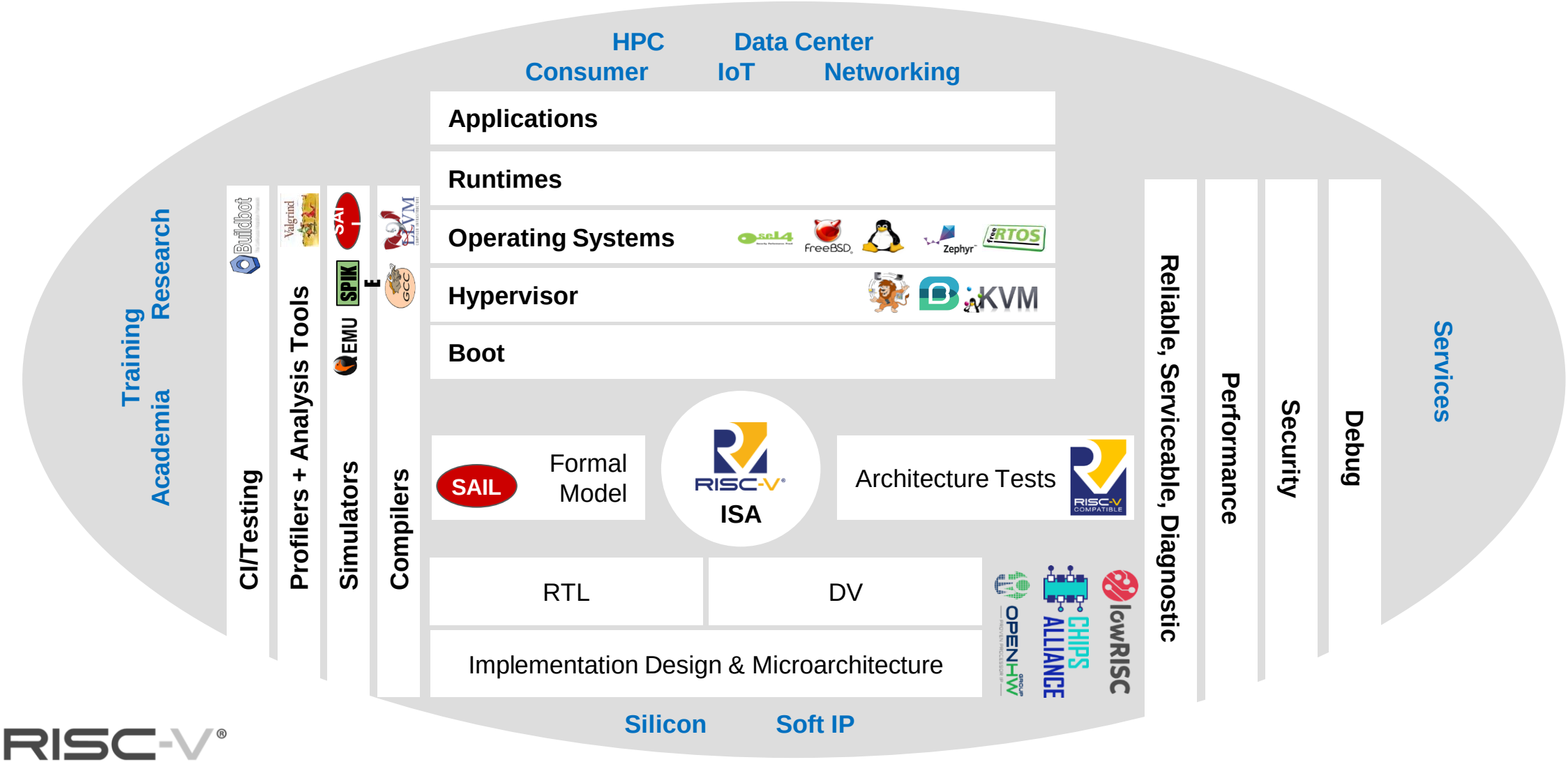
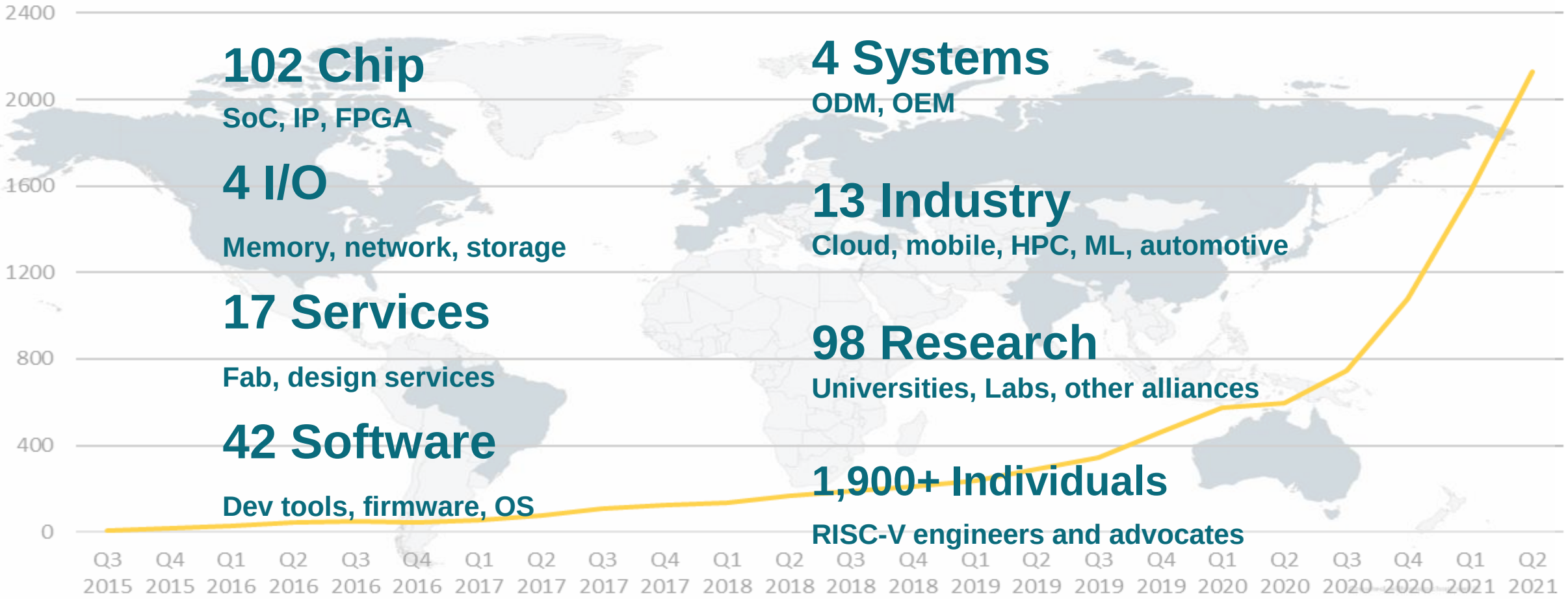
RISC-V®

RISC-V Ecosystem



More than 2,200 RISC-V Members

across 70 Countries



102 Chip

SoC, IP, FPGA

4 I/O

Memory, network, storage

17 Services

Fab, design services

42 Software

Dev tools, firmware, OS

4 Systems

ODM, OEM

13 Industry

Cloud, mobile, HPC, ML, automotive

98 Research

Universities, Labs, other alliances

1,900+ Individuals

RISC-V engineers and advocates

RISC-V membership grew 133% in 2020.
In 2021, RISC-V membership has already doubled.

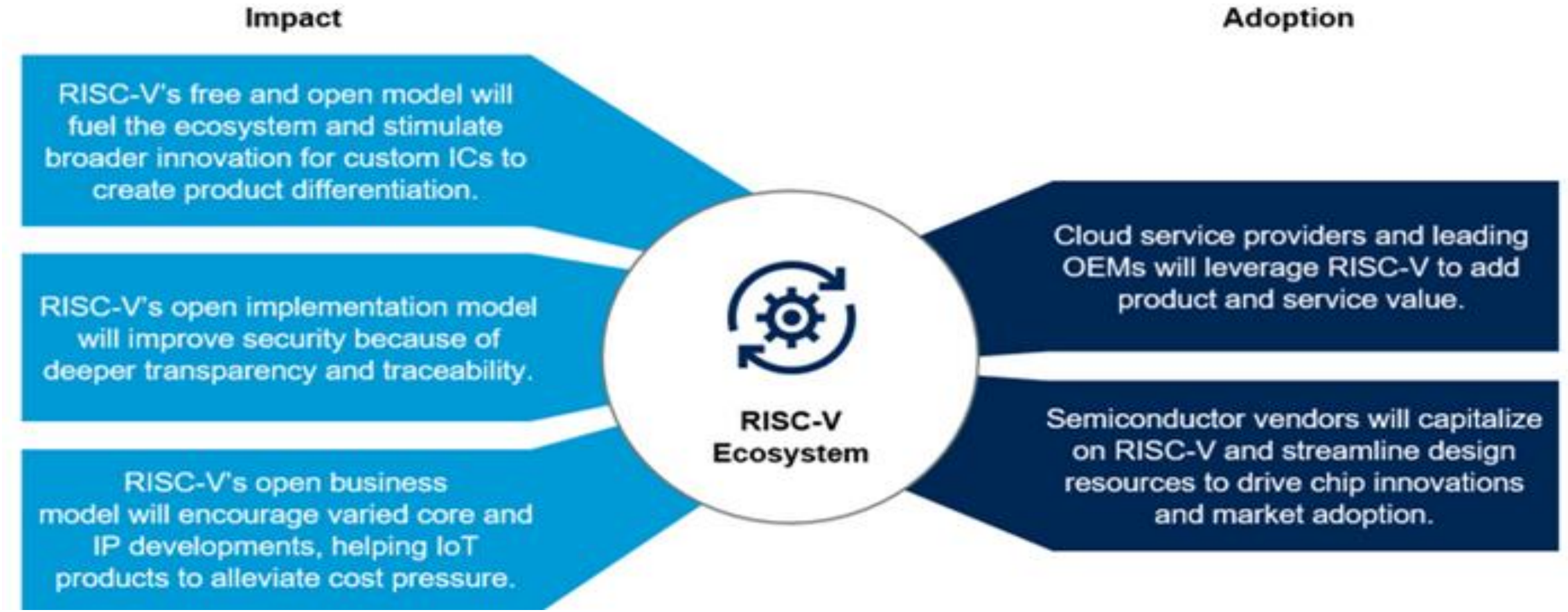
By 2025, 40% of application-specific integrated circuits (ASICs) will be designed by OEMs, up from around 30% today.

Custom ICs Based on RISC-V Will Enable Cost-Effective IoT Product Differentiation

Gartner, June 2020

Source: Gartner

RISC-V's open model will spur adoption by cloud service providers and streamline resources for chip vendors



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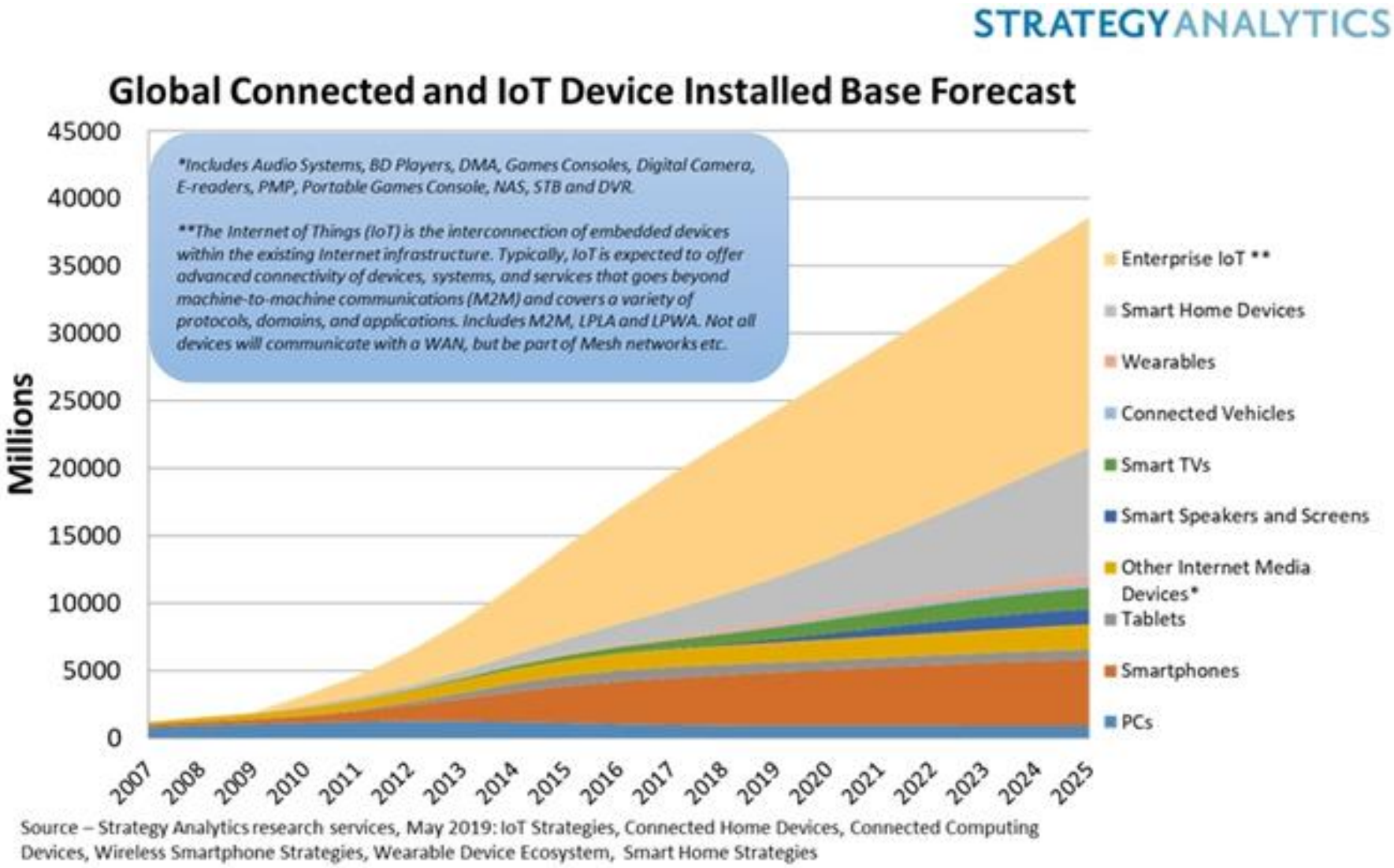
Source: Gartner
ID: 46523_C

50 billion connected and IoT devices

demand security and custom processors by 2030



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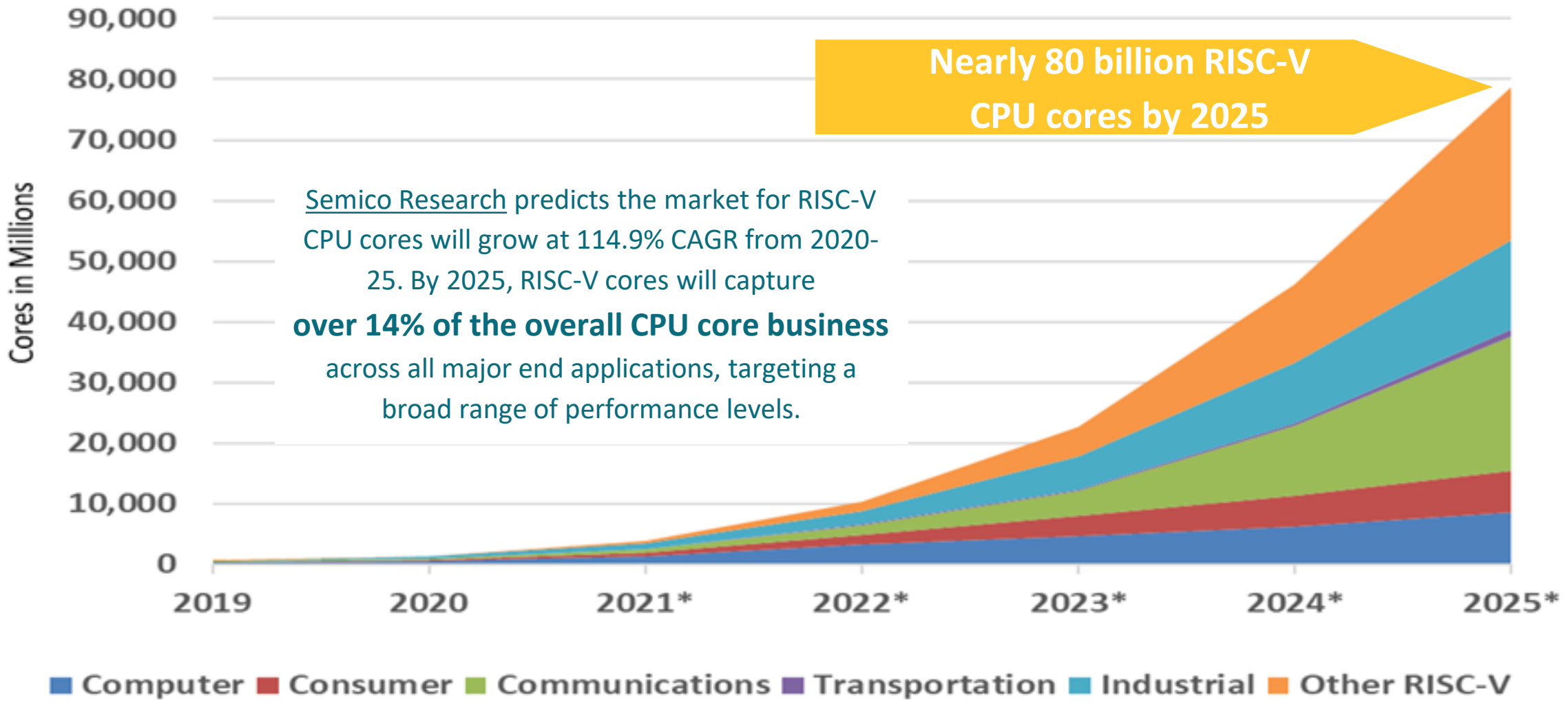
Source: Strategy Analytics

Rapid RISC-V growth led by industrial



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Source: Semico Research Corp. March 2021

RISC-V is the foundation of the Open era of computing

- **4k+ individuals in 60+ RISC-V work groups** and committees
- **330+ RISC-V solutions** online including cores, SoCs, software, tools, and developer boards
- **29 local RISC-V community** groups, with more than **5,400 engineers**
- We're in the news! We have **40k+ followers on social media** and across the last year, we have participated in **135+ news articles** along with amplifying RISC-V community news 450+ times.

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RISC-V Special Interest Group on HPC

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Special Interest Group – High Performance Computing SIG-HPC

https://lists.riscv.org/g/sig-hpc

SIG-HPC Vision & Mission: RISC-V: IoT to *HPC*

Vision:

The technical and strategic imperatives that guide the RISC-V ecosystem development to enable an Open HPC Ecosystem…

Mission:

…enable RISC-V in a broader set of new software and hardware opportunities in the High Performance Computing space, from the edge to supercomputers, and the software ecosystem required to run legacy and emerging (AI/ML/DL) HPC workloads.

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SIG-HPC: An Open era of HPC!

- CPUs, Accelerators, other hardware units, and coprocessors
- Verification and compliance infrastructure and methodologies specific to HPC
- Alignment and engagement and IP enablement.
- RISC-V software ecosystem alignment
- Engage and represent RISC-V in compute intensive industry and academic events
- Identify key industrial and academic partners.
- Support global technology independence with a RISC-V ecosystem roadmap and partners

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SIG-HPC Initiatives

- Guide and enable the community
  - Virtual Memory
    - SV57, SV57K, SV64, SV128
  - HPC SW & HW ecosystem & roadmap
  - Accelerators
  - ISA Extensions
  - **HPC Software Stack**
    - Starting with HPC Libraries

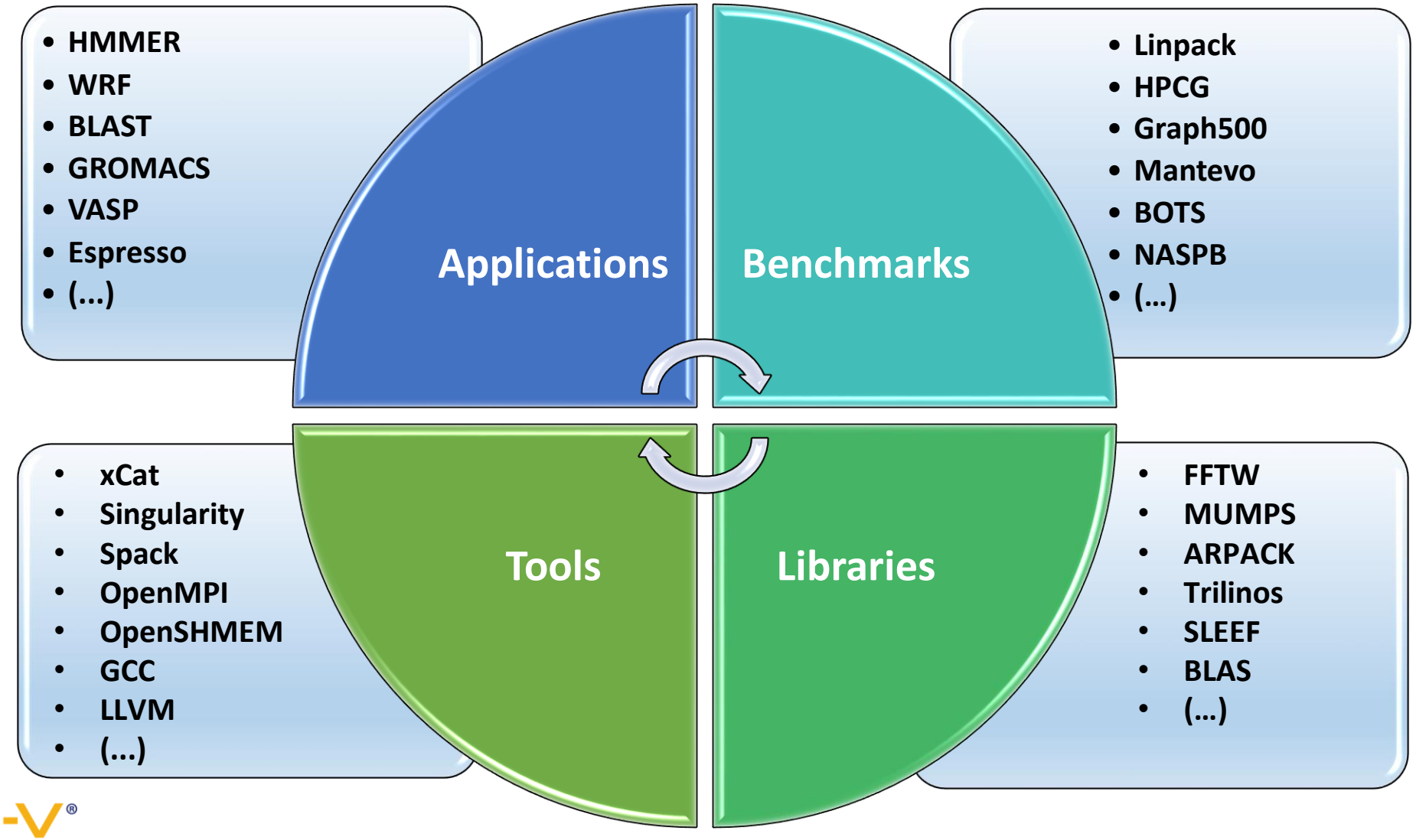
Tactical Computing Labs

HPC Software Testbed

John Leidel, Ph.D.

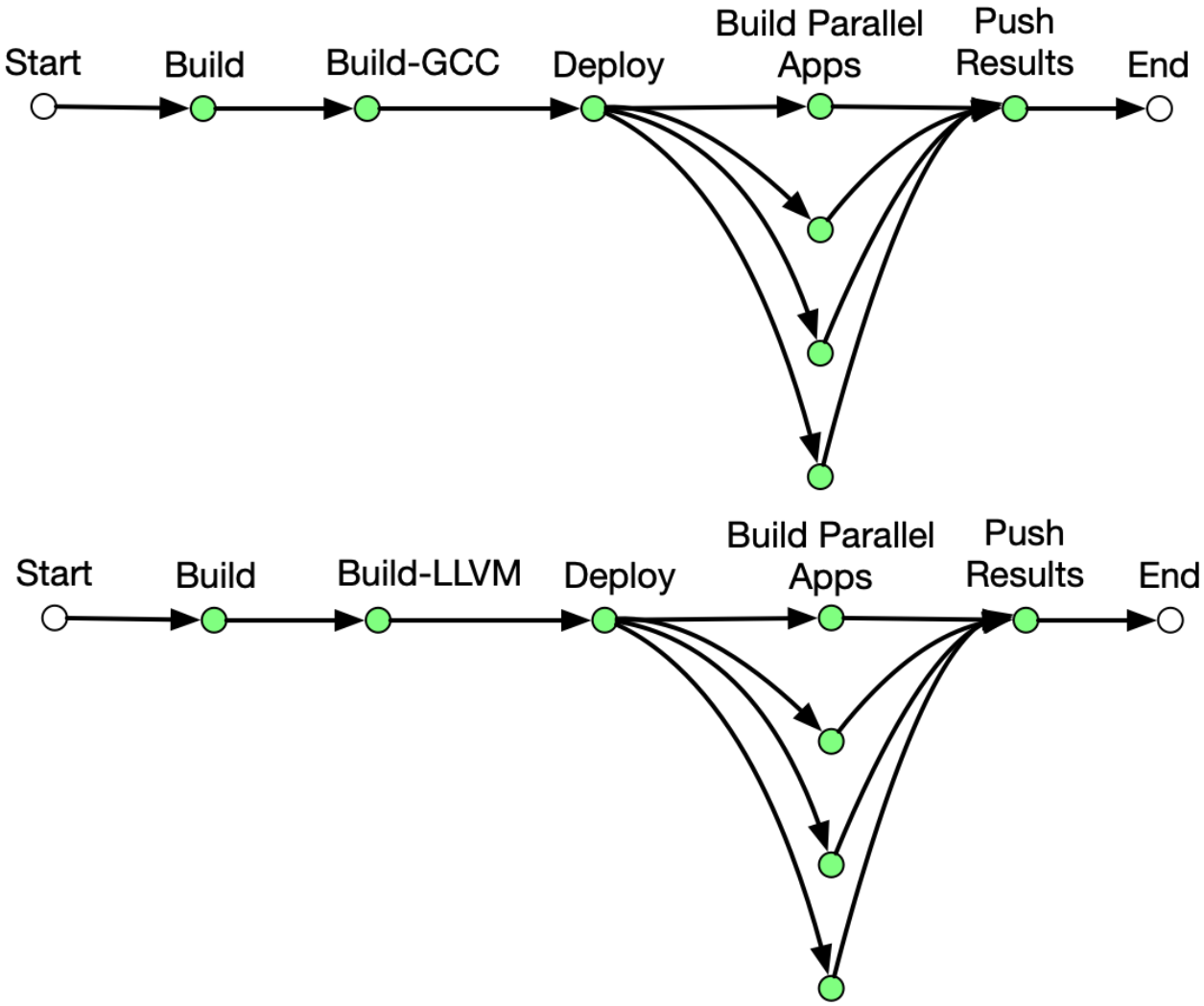
Tactical Computing Labs, RISC-V Technology HC Chair & SIG-HPC Co-Chair

Categories of Software



HPC Software Testbed

- We are working with the RISC-V International group to drive requirements for adjacent working groups
- RISC-V HPC Tests
  - HPC-centric software test suite
  - Multi-version compiler centric: GCC, LLVM
  - Using each compiler, we cross compile each target library, benchmark and application suite for RISC-V compatibility



HPC Software Testbed: riscv-test.org

RISC-V Test

All

S	W	Name ↓	Last Success	Last Failure	Last Duration
✓		llvm-project-11.0.0	6 days 12 hr - #38	7 mo 9 days - #1	37 min
✓		llvm-project-11.0.1	6 days 12 hr - #33	6 mo 15 days - #1	3 hr 51 min
✓		llvm-project-12.0.0	6 days 13 hr - #6	1 mo 0 days - #1	4 hr 18 min
✓		llvm-project-12.0.1	6 days 12 hr - #5	N/A	4 hr 15 min
✓		llvm-project-master	6 days 12 hr - #62	1 mo 4 days - #58	7 hr 20 min
✓		riscv-gnu-toolchain-master	6 days 12 hr - #60	5 mo 21 days - #36	2 hr 47 min

Icon: S M L

Legend Atom feed for all Atom feed for failures Atom feed for just latest builds

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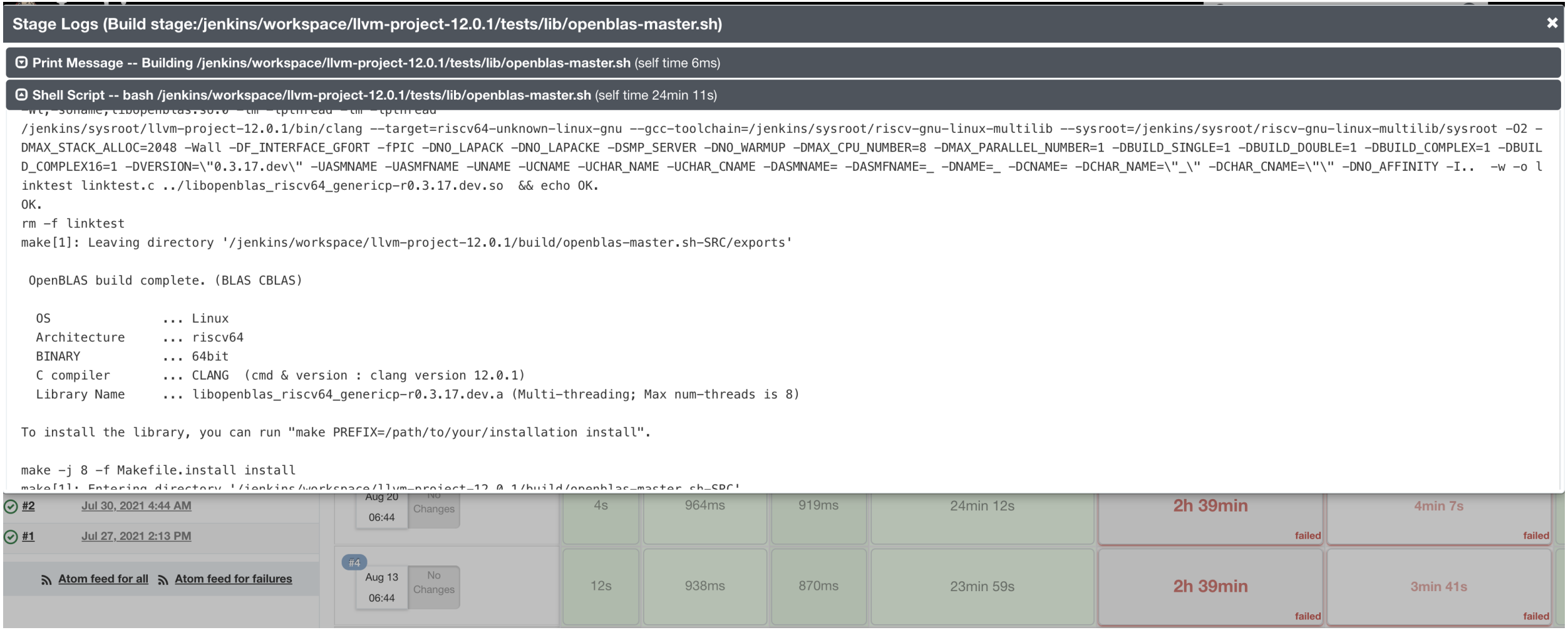
HPC Software Testbed: Public Results



Public Test Harness

- The results are public!
  - https://riscv-test.org/
- The test harness has been created in a public Github repo
- https://github.com/riscv-test/riscv-hpc
- The harness includes a set of template scripts for each test
  - Each test pulls it own source code (archive or Git repo)
  - Unpacks the source, configures it and builds it
  - Adding tests is as simple as adding scripts to the Github repository
- The top-level harness provides common access to:
  - Directory structures
  - Compiler paths
  - Compiler flags
- **Pull requests are encouraged!**

riscv-hpc

license BSD

This repository serves as the basis for the official RISC-V HPC test suite that is executed via the Jenkins CI host at https://riscv-test.org.

License

The RISC-V HPC test suite is licensed under a BSD-style license - see the LICENSE file for details.

Architecture Overview

The RISCV-HPC test architecture is setup specifically to support testing various compilers, libraries benchmarks and applications for high performance computing against the RISC-V software ecosystem.
The test architecture is crafted specifically to support inclusion of a variety of different software tools that can be built using different compilers and/or compiler versions. Note that these software entities are NOT executed. We do not execute and/or track benchmark performance of any software package, benchmark or application. Rather, this infrastructure is designed to find the gaps in the RISC-V software ecosystem.

As we see in the figure below, the test infrastructure is crafted using a series of build scripts integrated into a Jenkins pipeline. Each pipeline instance is initiated at a specific cadence (documented in the Jenkins environment). The first stage of the pipeline initializes the test environment. The second stage of the pipeline initializes a set of global variables that are utilized by individual test scripts. These global variables initialize values such as the absolute installation path of the target compiler, the required compiler flags and other various paths. The third stage of the pipeline builds the target compiler. For compilers that are designated as "release" builds, we utilize a previously built compiler (as release builds rarely change).
For compiler builds that target the top of tree source code, we build and install the entire compiler from scratch. Once the compiler build has been deemed stable, we execute three sets of nested pipeline stages. The first stage builds and installs candidate libraries. This can be from release archives or from top-of-tree git repositories. We

Building an Open HPC Ecosystem with RISC-V

- HPC requires customized hardware solutions for many HPC domains
- HPC is tackling grand challenges that benefit from the Global Technology ecosystem
- HPC is on the technology leading edge

- An Open ISA complements Open Source Software and combines to create an open Ecosystem

- RISC-V accelerates innovation both in Research and Industry
- The RISC-V community and ecosystem are rapidly growing

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HPC Software stack @ BSC

- Clusters:

Board	OS	Details
PolarFire	Fedora	4 cores w/ 2 GB
BeagleV	Fedora	2 cores w/ 8 GB
Unmatched	Fedora/Ubuntu	4 cores w/ 16 GB
Allwinner D1 (Vector extension)	Fedora	1 core w/ 2 GB

- RISC-V Software Stack:
  - Linux, SLURM
  - Compilers:
    - go/1.17
    - openmpi/fedora/4.1.1_gcc10.3.1
    - llvm/EPI-0.7-development
    - openmpi/ubuntu/4.1.1_gcc10.3.0
    - llvm/EPI-development
    - python/fedora/2.7.16
  - Tools
    - extrae/3.8.3
    - papi/6.0.0
    - perf/5.11.10
    - singularity/3.8.2
  - Libraries
    - boost/1.77.0
    - glibc/fedora/2.33
    - openBLAS/0.3.15
    - fftw/3.3.9_gcc10.3.1_ompi4.1.1
    - libunwind/git
    - openBLAS/0.3.17

You Can Help

- Get involved in SIG HPC
- https://lists.riscv.org/g/sig-hpc
- Subscribe:
  - Send email to: sig-hpc+subscribe@lists.riscv.org
- Monthly meetings
  - 3rd Thursday of the month
  - Next meeting: February 17th @ 16:00 CET

Getting Started

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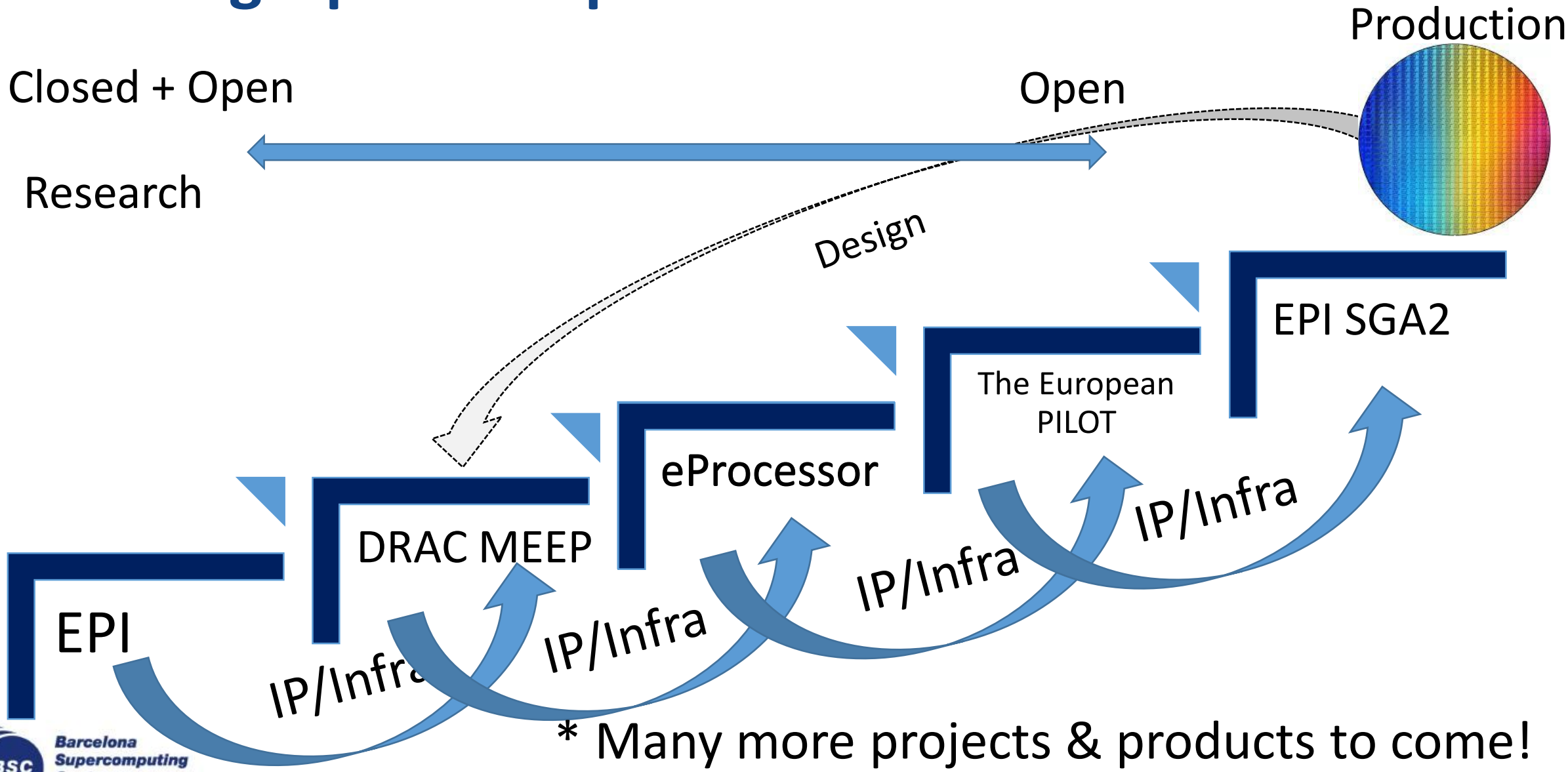
Building Open European HPC CPUs & Accelerators



Playing with RISC-V

- QEMU
  - Software emulator
  - Getting Started Guides:
    - https://wiki.ubuntu.com/RISC-V
    - https://fedoraproject.org/wiki/Architectures/RISC-V/Installing
  - EasyBuild on QEMU (from Kenneth Hoste)
    - https://gist.github.com/boegel/6530823d57629b69aa3b0384870fdd8d
      - Some of that is quite specific to Gentoo

- Development Boards
  - Several that you can buy: https://riscv.org/exchange/boards/

Q&A

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Thank you

john.davis@bsc.es